CLAIMS

What is claimed is:

1. A programmable logic device (PLD) that facilitates the use of triple modular redundancy (TMR), the PLD comprising:

a plurality of programmable logic blocks;

a plurality of interconnect lines; and

a plurality of programmable routing multiplexer circuits programmably interconnecting the interconnect lines with each other and with the programmable logic blocks,

wherein each programmable routing multiplexer circuit comprises:

a plurality of multiplexer input terminals;

a multiplexer output terminal;

a plurality of configuration memory cells; and

a plurality of unidirectional logic circuits, each unidirectional logic circuit having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and a control terminal coupled to an output terminal of an associated configuration memory cell.

2. The PLD of Claim 1, wherein:

a first programmable logic block is programmed to implement at least a portion of a first TMR module;

a second programmable logic block is programmed to implement at least a portion of a second TMR module; and

one of the programmable routing multiplexer circuits has a first multiplexer input terminal coupled to an output terminal of the first programmable logic block and a second multiplexer input terminal coupled to an output terminal of the second programmable logic block.

3. The PLD of Claim 1, wherein each unidirectional logic circuit comprises a unidirectional buffer and a pass gate coupled in series between the associated multiplexer input terminal and the multiplexer output terminal, the pass gate having a gate terminal coupled to the output terminal of the associated configuration memory cell.

4. The PLD of Claim 3, wherein the pass gates comprise N-channel transistors.

5. The PLD of Claim 3, wherein the unidirectional buffer is a non-inverting buffer.

6. The PLD of Claim 1, wherein each unidirectional logic circuit comprises a tristate buffer having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and an enable terminal coupled to the output terminal of the associated configuration memory cell.

7. The PLD of Claim 6, wherein the tristate buffer is an inverting buffer, and each of the programmable routing multiplexer circuits further comprises an inverting output buffer having an input terminal coupled to the multiplexer output terminal.

8. The PLD of Claim 1, wherein each of the programmable routing multiplexer circuits further comprises an output buffer having an input terminal coupled to the multiplexer output terminal.

9. The PLD of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

10. The PLD of Claim 1, wherein each programmable routing multiplexer circuit comprises eight multiplexer input terminals, eight configuration memory cells, and eight unidirectional logic circuits.

11. The PLD of Claim 1, wherein each programmable routing multiplexer circuit further comprises an output buffer coupled between the output terminals of the unidirectional logic circuits and the multiplexer output terminal.

12. A system controlled by memory cells susceptible to single event upsets (SEUs), the system comprising:

a plurality of logic circuits;

a plurality of interconnect lines; and

a plurality of programmable routing multiplexer circuits programmably interconnecting the interconnect lines with each other and with the logic circuits,

wherein each of the programmable routing multiplexer circuits comprises:

a plurality of multiplexer input terminals;

a multiplexer output terminal;

a plurality of memory cells susceptible to SEUs; and

a plurality of unidirectional logic circuits, each unidirectional logic circuit having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and a control terminal coupled to an output terminal of an associated memory cell.

13. The system of Claim 12, wherein:

a first logic circuit implements at least a portion of a first TMR module;

a second logic circuit implements at least a portion of a second TMR module; and

one of the programmable routing multiplexer circuits has a first multiplexer input terminal coupled to an output terminal of the first logic circuit and a second multiplexer input terminal coupled to an output terminal of the second logic circuit.

14. The system of Claim 12, wherein each unidirectional logic circuit comprises a unidirectional buffer and a pass gate coupled in series between the associated multiplexer input terminal and the multiplexer output terminal, the pass gate having a gate terminal coupled to the output terminal of the associated configuration memory cell.

15. The system of Claim 14, wherein the pass gates comprise N-channel transistors.

16. The system of Claim 14, wherein the unidirectional buffer is a non-inverting buffer.

17. The system of Claim 12, wherein each unidirectional logic circuit comprises a tristate buffer having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and an enable terminal coupled to the output terminal of the associated memory cell.

18. The system of Claim 17, wherein the tristate buffer is an inverting buffer, and each of the programmable routing multiplexer circuits further comprises an inverting output buffer having an input terminal coupled to the multiplexer output terminal.

19. The system of Claim 12, wherein each of the programmable routing multiplexer circuits further comprises an output buffer having an input terminal coupled to the multiplexer output terminal.

20. The system of Claim 12, wherein the system comprises a programmable logic device (PLD).

21. The system of Claim 20, wherein the PLD is a field programmable gate array (FPGA).

22. The system of Claim 12, wherein each programmable routing multiplexer circuit comprises eight multiplexer input terminals, eight memory cells, and eight unidirectional logic circuits.

23. The system of Claim 12, wherein each programmable routing multiplexer circuit further comprises an output buffer coupled between the output terminals of the unidirectional logic circuits and the multiplexer output terminal.

24. A programmable routing multiplexer circuit, comprising:

a plurality of multiplexer input terminals;

a multiplexer output terminal;

a plurality of configuration memory cells; and

a plurality of unidirectional logic circuits, each unidirectional logic circuit having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and a control terminal coupled to an output terminal of an associated configuration memory cell.

25. The programmable routing multiplexer circuit of Claim 24, wherein:

a first multiplexer input terminal is coupled to a first TMR module; and

a second multiplexer input terminal is coupled to a second TMR module.

26. The programmable routing multiplexer circuit of Claim 24, wherein each unidirectional logic circuit comprises a unidirectional buffer and a pass gate coupled in series between the associated multiplexer input terminal and the multiplexer output terminal, the pass gate having a gate terminal coupled to the output terminal of the associated configuration memory cell.

27. The programmable routing multiplexer circuit of Claim 26, wherein the pass gates comprise N-channel transistors.

28. The programmable routing multiplexer circuit of Claim 26, wherein the unidirectional buffer is a non-inverting buffer.

29. The programmable routing multiplexer circuit of Claim 24, wherein each unidirectional logic circuit comprises a tristate buffer having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and an enable terminal coupled to the output terminal of the associated configuration memory cell.

30. The programmable routing multiplexer circuit of Claim 29, wherein the tristate buffer is an inverting buffer, and the programmable routing multiplexer circuit further comprises an inverting output buffer having an input terminal coupled to the multiplexer output terminal.

31. The programmable routing multiplexer circuit of Claim 24, wherein the programmable routing multiplexer circuit further comprises an output buffer having an input terminal coupled to the multiplexer output terminal.

32. The programmable routing multiplexer circuit of Claim 24, wherein the programmable routing multiplexer circuit comprises eight multiplexer input terminals, eight configuration memory cells, and eight unidirectional logic circuits.